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DIGITAL TWIN BASED UNCERTAINTY INFORMED TIME CONSTRAINT CONTROL IN SEMICONDUCTOR MANUFACTURING

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ABSTRACT

Semiconductor manufacturing, commonly described as a complex job shop, contains product-inherent constraints that amplify dispatching complexities. Most notably time constraints restrict the maximum waiting time between processes inducing the need to control the release of time constraint lots as violations lead to scrap. The proposed approach uses a fab wide digital twin in form of discrete event simulation based on knowledge graph structure and derives uncertainty informed time constraint violation probabilities through rollouts in near real time. A real-world front end semiconductor manufacturing fab serves as an ex-post validation and shows the benefits of the approach.

1 INTRODUCTION

The importance and growth of the electronics industry has been for the past few years stimulated by massive, global trends, such as , Artificial Intelligence (AI), Internet of Things (IoT), Natural Language Processing and smart products and the software-defined characteristics of modern systems (May et al. 2022). As a consequence, the electronics industry has become one of the largest industries world-wide as semiconductors are essential components in all industries nowadays (Maleck and Eckert 2017). Embedding circuits into new product generations is critical for dealing with climate change and resource scarcity (Uçar et al. 2020). Therefore, semiconductors enable the achievement of energy efficiency, individual mobility, security, the establishment of Industrial Internet of Things (IIoT) and the application of AI. This has led to fast innovation cycles in semiconductor manufacturing and thus its technology-intensive and capital-intensive nature (Mönch et al. 2011). The technological intensity is manifested in the presence of forming and cutting processes, electro-physical and chemical processes, abrasive processes, surface engineering and metrology augmented by complex machinery and production system organization as well as highly specialized semiconductor design (Mönch et al. 2013). The maximization of the material potential and avoiding the production of faulty products is crucial and, for that reason, semiconductor manufacturing equipment accounts for a major cost driver (Hong et al. 2023). Hence, in so called fabs, short for semiconductor fabrication plants, operate any day for the whole day. To minimize coordination effort and setup times wafers containing Integrated Circuit (IC) chips are packetized into lots of 25 or 50 (Ziarnetzky et al. 2017). Furthermore, it is necessary to often visit several machines to transform semiconductor material into an IC in a layer by layer manner leading to recurrent material flow (Altenmüller et al. 2020). Beyond individual technological complexity the major challenge for semiconductor manufacturing lies in the coordination of this complex job shop (Mönch et al. 2011). Each wafer, a thin slice of semiconductor material, requires up to 800 processing steps each between a few minutes and several hours (Ziarnetzky et al. 2017). Maintaining the yield high is decisive. In addition to processing or design errors a major yield loss consists of contaminated wafers through native oxidation, crystal formation, ion migration or dust deposition (Lima et al. 2021). These impurities pollute the surface and inhibit the designed electrical flow. Thus, semiconductor manufacturing equipment in fabs is operated in clean rooms to reduce contamination (Klemmt and Mönch 2012). Nevertheless, between many process steps wafers can only remain unprocessed for several hours otherwise yield is reduced as the wafers can often not be recovered and have to be scrapped

(Altenmüller et al. 2020). Hence, adhering to these time constraints is of utmost importance (Arima et al. 2015). System behavior is time transient as the overall time wafers spend within a fab can be up to several weeks and months due to the recurrent material flow (Mönch et al. 2013). Controlling the production under time constraints, re-entrant and non-linear material flow given varying process times is challenging (Wang et al. 2018). Additionally, the process is time-consuming and stressful for operators (Lima et al. 2017b). In this volatile environment production control is amplified by human operators that deal with time constraints (Lima et al. 2019). This requires extra, manually made, effort, that is error-prone, inconsistent and does not optimize opportunities. Making use of the real-time fab data can enable overcoming traditional, rule-based approaches that are too rigid (Altenmüller et al. 2020). Establishing an intelligent, digital twin based production control in this complex job, that minimize time constraints violations, can alleviate the current shortcomings. Additionally, reducing these wasteful activities not only contributes to monetary business objectives, operator well-being, but also to sustainability and the achievement of net zero climate goals as wafer fabrication is energy intensive (May et al. 2021).

2 LITERATURE REVIEW

Time constraints limit the maximum time for an individual lot between completing processing of operation *A* and starting operation *B*, where *A,B,...* defines the ordered list of operations to be performed on the particular lot (Klemmt and Mönch 2012). As visualized in Figure 1 simple time constraints regard two consecutive operations *A, A+1*, while timelink area constraints regard non-consecutive operations. Through consecutive or nested time constraints the complexity for production control can be increased (Wang et al. 2018). Thus, most studies restrict themselves to simple time constraints (Altenmüller et al. 2020).

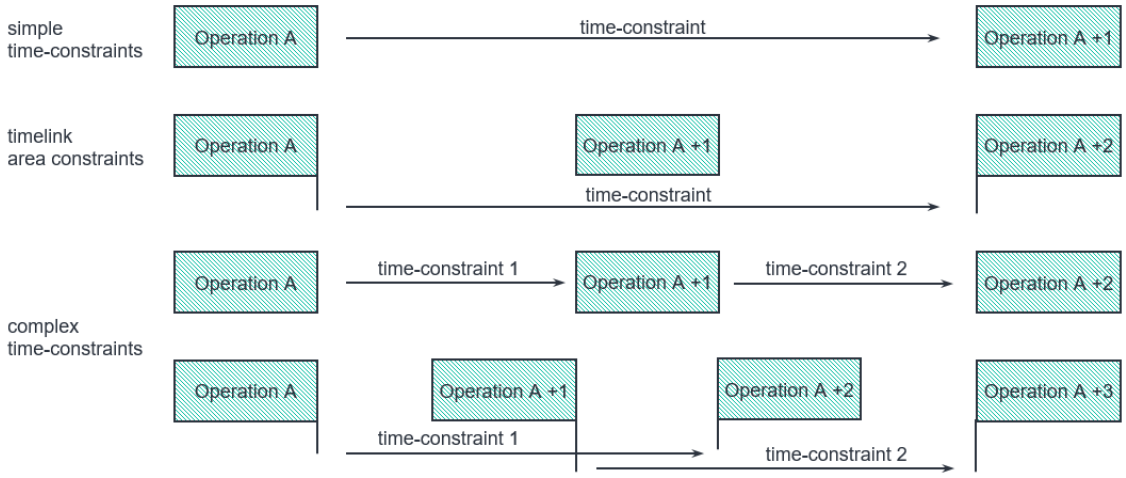

Figure 1: Time constraint types based on (Klemmt and Mönch 2012); (Wang et al. 2018).

Dealing with time constraints by aiming at a minimization of time constraint violations through various levers is a decade old journey (Klemmt and Mönch 2012). It is aggravated with increasingly smaller dimensions that put even more stringent time limits on time constraints. On a capacity planning level (Robinson and Giglio 1999) proposed a queuing theory based time constraint violation probability prediction. Given a specific yield target the optimal number of machines and the associated low violation probability can be obtained. These approaches can be extended to include machine breakdowns (Tu and Chen 2009) or batch equipment (Tu and Chen 2011) and yield a concrete increase in capacity due to the time constraints. As opposed to a simulation approach that aimed at experimentally verifying the influence of different time constraints in semiconductor manufacturing capacity planning, which found that both frequency and time limit have a strong influence on the effects of fab performance (Pappert et al. 2016). A real world machine learning based approach that predicts inventory levels confirmed these results (Chien et al. 2020).

These influences however cannot be appropriately addressed in capacity planning, so that time constraint adherence must be ensured on an operational level (Ono et al. 2006).

Operational control of time constraints is achieved through scheduling or dispatching. The former is widely regarded in literature as it has an abstract, prescriptive nature, is falling in line with traditional fab planning and control as well as the low complexity of dispatching rules applied in real world use cases (Bixby et al. 2006). The main disadvantage of using scheduling, in particular MILP exact solutions, is their limit to two (An et al. 2016), three (Kim and Lee 2017) or in general few machines with 20 to 30 jobs to be scheduled (Yu et al. 2013). Constraint programming can increase the production scale in real world applications (Maleck and Eckert 2017), yet is still limited to areas within a complex job shop (Maleck et al. 2018). Through decomposition these approaches can effectively reduce the average number of time constraint violations (Maleck et al. 2019). To speed up the optimization (Zhou and Wu 2017) propose simulated annealing, that can be extended to regard larger problem settings (Nattaf et al. 2019). However, further extensions with cuckoo search still cannot control entire fabs (Zhou et al. 2019). Oftentimes in semiconductor fab scheduling studies time constraints are not directly regarded but only secondarily profit from reduced cycle times (Lee 2020). One approach in control of a fab uses a related approach that is based on a blacklist and whitelist to select possible lots with time constraints (Winkler et al. 2016). The authors propose a nested simulation model where over a prescribed period individual decisions are taken, which itself are validated in one simulation. The results however are not uncertainty informed as only an individual rollout of a simplified simulation, to avoid the real system complexities, is performed.

On a dispatching level priority rules, heuristics, are the predominant form of controlling material flow in semiconductor manufacturing (Altenmüller et al. 2020). Hence, it is no wonder earliest applications in dispatching study the influence of heuristics and their input to reduce time constraint violations (Scholl and Domaschke 2000). Using these simulations to identify and deduce good heuristics (Zhang et al. 2016), carefully prioritize time constraint lots (Kobayashi et al. 2013) or optimize a rule-based dispatching including criticalities (Kopp et al. 2020) and product-mix (Toyoshima et al. 2013) is widely applied. These studies, however, show, that higher fidelities of simulations give rise to more situational awareness and improved dispatching decisions with respect to time constraint violations (Ciccullo et al. 2014). Within such simulation (Altenmüller et al. 2020) train a deep reinforcement learner to dispatch lots and adhere to time constraint, which is extended by (Valet et al. 2022) who control dispatching and maintenance simultaneously. Thus, the notion of a gate keeping decision in dispatching to avoid dispatching lots with critical time constraints is predominant (Pirovano et al. 2020). For controlling this particular decision heuristic control policies can be derived (Wu et al. 2016). Alternatively, (Sadeghi et al. 2015) present an approach to estimate the time constraint adherence probability by schedule randomization and comparison and evaluation. An improved intelligent sampling approach is presented by (Lima et al. 2017a) and extended to cover full semiconductor fabs (Lima et al. 2017b) and ultimately recognize more complex grouping (Lima et al. 2021). In a similar vein, yet training a machine learning predictor on past real-world fab data, (May et al. 2021) propose uni- and multi-variate time series predictors to evaluate the time constraint violation probability or use future machine tool queue predictions as approximations (May et al. 2021). The extended approach shows significant improvements in avoiding time constraint violations in real-world semiconductor fabs (May et al. 2021). Using simulations not only to validate the proposed dispatching or gate keeping policies but to evaluate the probability of time constraint violations has not been regarded.

Thus, the application of digital twins, up-to-the-minute instantiated high fidelity discrete event simulations of a semiconductor fab, to control time constraint adherence in a semiconductor fab can bridge the gap between simulation and data-based approaches. Thereby the time constraint violation probability refers to an uncertainty aware evaluation of time constraints adherence of an individual lot in the binary domain. This leads to the following two research questions: First, how can a digital twin architecture be derived that can be used to obtain time constraint violation predictions from observation of the digital twin behavior? Second, how can such a digital twin and violation prediction be used to reduce time constraint violations in an actual wafer fab?

3 DIGITAL TWIN ARCHITECTURE

A digital twin on a production system level can be described as a discrete event simulation (DES) that can transform manual, intuition based processes to a data-based, clearly described fictional system (Uhlemann et al. 2017). Extending this notion (Negri et al. 2017) envision synchronized simulations on different levels to constitute a digital twin. By evaluating the performance of various control policies in near real-time in the digital twin a foresighted digital twin is constructed (May et al. 2021). Beyond traditional manufacturing and semiconductor fabs the concept of coupling a digital twin with real-time predictions and control has been successfully shown in a petrochemical factory (Min et al. 2019). In the realm of semiconductor fabs the flexibility of the simulation model to accommodate for the large variety of equipment and constraints has shown beneficial (Valet et al. 2022). One particular approach can serve as the blueprint for such a flexible digital twin architecture that is capable of describing such systems, an ontology, knowledge-graph based DES (May et al. 2022). The system is modeled as an instantiated knowledge graph that conforms to an ontology describing the potential interrelations of such a real-world system. Due to this graph like structure the simulation is serialized per se and changes are immediately reflected in the knowledge graph, the core of the simulation. To apply randomization and apply it in large scale in a full semiconductor fab at speed the following digital twin architecture is derived.

3.1 DES System Elements

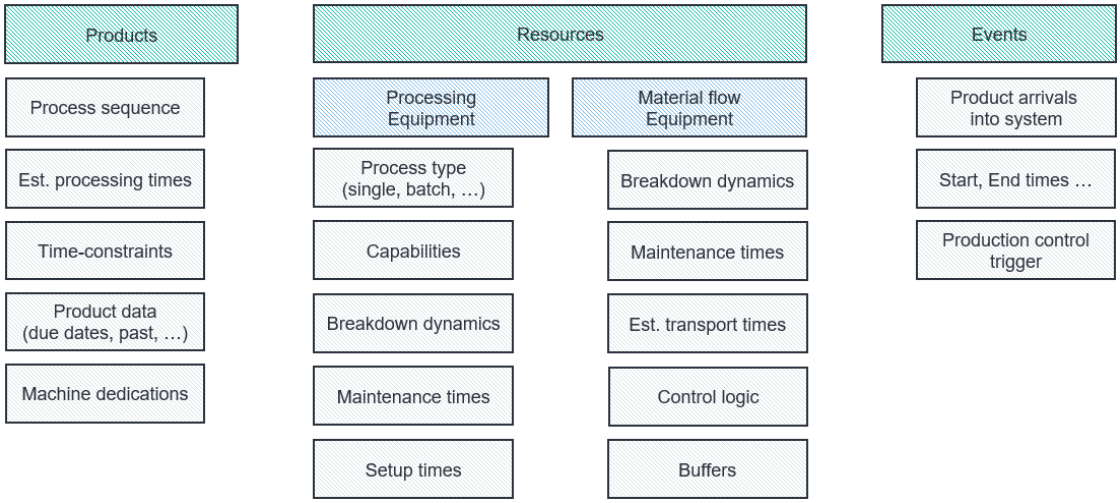

Figure 2: Relevant simulation system elements.

First, based on the OntologySim (May et al. 2022) and previous semiconductor manufacturing system simulations (Kuhnle et al. 2022) required system elements are derived and divided into products, i.e. lots in fabs, resources, in particular processing equipment and transporting equipment relevant for material flow, as well as events to constitute a discrete event simulation. Given expert knowledge and data analysis with respect to queues and time constraints in semiconductor fabs (May et al. 2021), (Mönch et al. 2011) ,(Lima et al. 2021) the simulation system elements are extended as visualized in Figure 2.

The structure of the knowledge graph is based on the ontology used in the OntologySim and extended towards semiconductor specifics. It can be visualized on a general structure of relevant elements for a generic system simulation as in Figure 3. All system elements are hence connected in form of a knowledge graph where vertices describe above mentioned entities and the interrelations are modeled through edges in a similar vein to the OntologySim (May et al. 2022). While process sequence, time constraints and product data can be directly obtained from the fab's database, processing times need to be estimated on

past long-term data. Equipment breakdown dynamics, maintenance and setup times have to be similarly calculated from past data. Regarding the system control either an integration of the existing control system to the digital twin is necessary or the control logic has to be reconstructed based on past behavior (May et al. 2024). Running the simulation model in the DES as a digital twin besides the real-world long-term data requires a short-term, real-time transfer of events to capture the current system status. Due to the knowledge graph based structure a direct transfer from the fab's real-time data can provide the initial starting point for the digital twin.

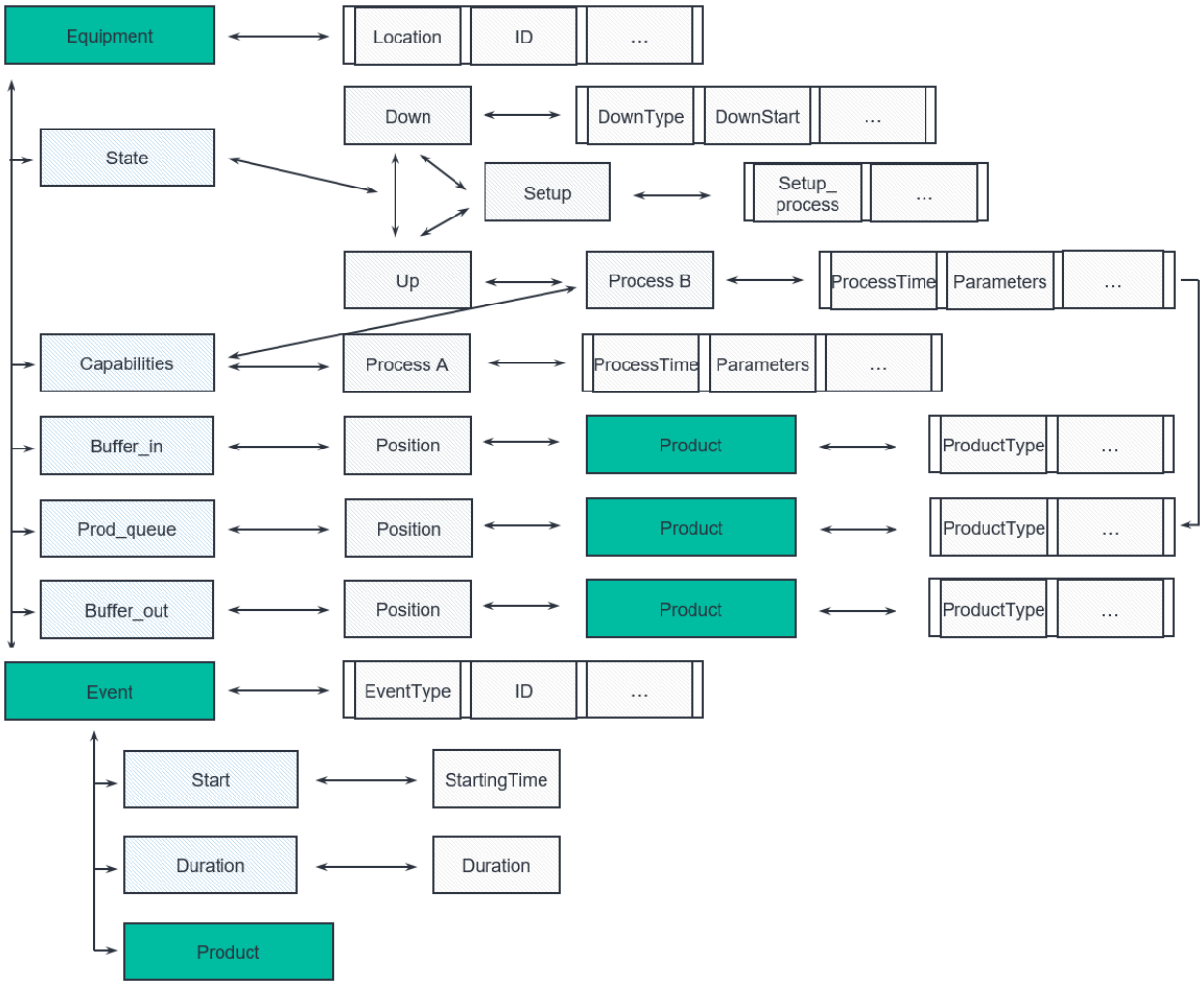

Figure 3: Selection of Knowledge Graph elements and structure based on (May et al. 2022).

3.2 Digital Twin Instantiation

To facilitate the digital twin architecture it is desirable to construct a model of the real system that in real time contains the current location, status and control of entities in the knowledge graph based structure that is also used in the DES. This constitutes a real-time data representation, often referred to as the digital shadow, and is used to instantiate the digital twin that can the be used to improve control (May et al. 2021). The overall structure is visualized in Figure 4 and contains the real-time system model as the digital representation which is instantiated to the digital twin.

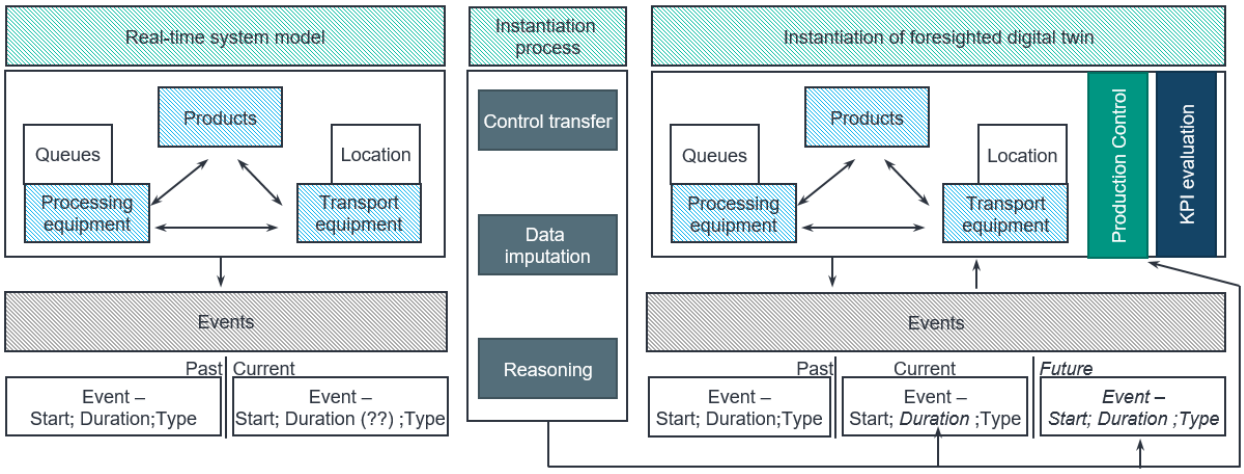

Figure 4: Digital twin architecture based on knowledge graph based DES and instantiation.

Constructing the digital representation makes use of fitting statistical distributions to observed past data. Within this study the detailed availability of real-time data from the fab's data based is not unlimited and, thus, constitutes the length of the observations regarded. Finding the perfect length of such a period is out of the scope of this study. In a similar vein past data can be mined to re-create the current status of lots, equipment and their interrelation provided sufficient data is available. The latter is used for the ex post evaluation so that the digital representation can serve as the up-to-the-minute model of the real system at any time.

Control transfer is not possible in form of interconnecting to the real control system in the course of this study. However, as only simple time constraints are regarded the evaluation time of one time constraint hardly exceeds a single day. Therefore, only short-term dispatching and scheduling have to be regarded. This can be even narrowed down as the evaluation task of the instantiated digital twin ends with a binary evaluation whether or not a time constraint within the simulation has been violated. Thus, the actual order in queues in positions after the lot in question would only be relevant in certain edge cases. This reduces the complexity and priority rules can be easily re-implemented and selected according to their actual fab usage at times. Missing data, in particular about current events, e.g. the duration and hence end of a current process for a certain lot, can imputed based on past data and the distributions mined. Due to the structure of a knowledge graph that corresponds to a pre-described ontology the model can be used for reasoning, which can identify missing links in new routings that have not been observed in the past, e.g. dedication of particular operations to certain machines.

4 TIME CONSTRAINT VIOLATION PREDICTION

To predict the violation of individual time constraints at the time the gate keeping decision of releasing or not releasing the time constraint lot is taken, the digital twin can be instantiated and the violation or adherence observed in the DES. The individual observation of a time constraint adherence however is insufficient to properly asses that violation probability (Lima et al. 2021). Thus, the digital twin is rolled out in a monte carlo style for multiple instances leading to an observation of the time constraint violations. The rollout strategy varies the seeds and scenarios obtained in the individual DES digital twin instances, to regard a more complete picture of the behavior as visualized in Figure 5. Multiple time constrained lots at the same gate keeping decision can similarly be evaluated. Production control decisions such as dispatching are taken by the transferred control logic as discussed in section 3, while later selection of time constrained lots are randomized to avoid an endless simulation of the proposed decision model in a simulation.

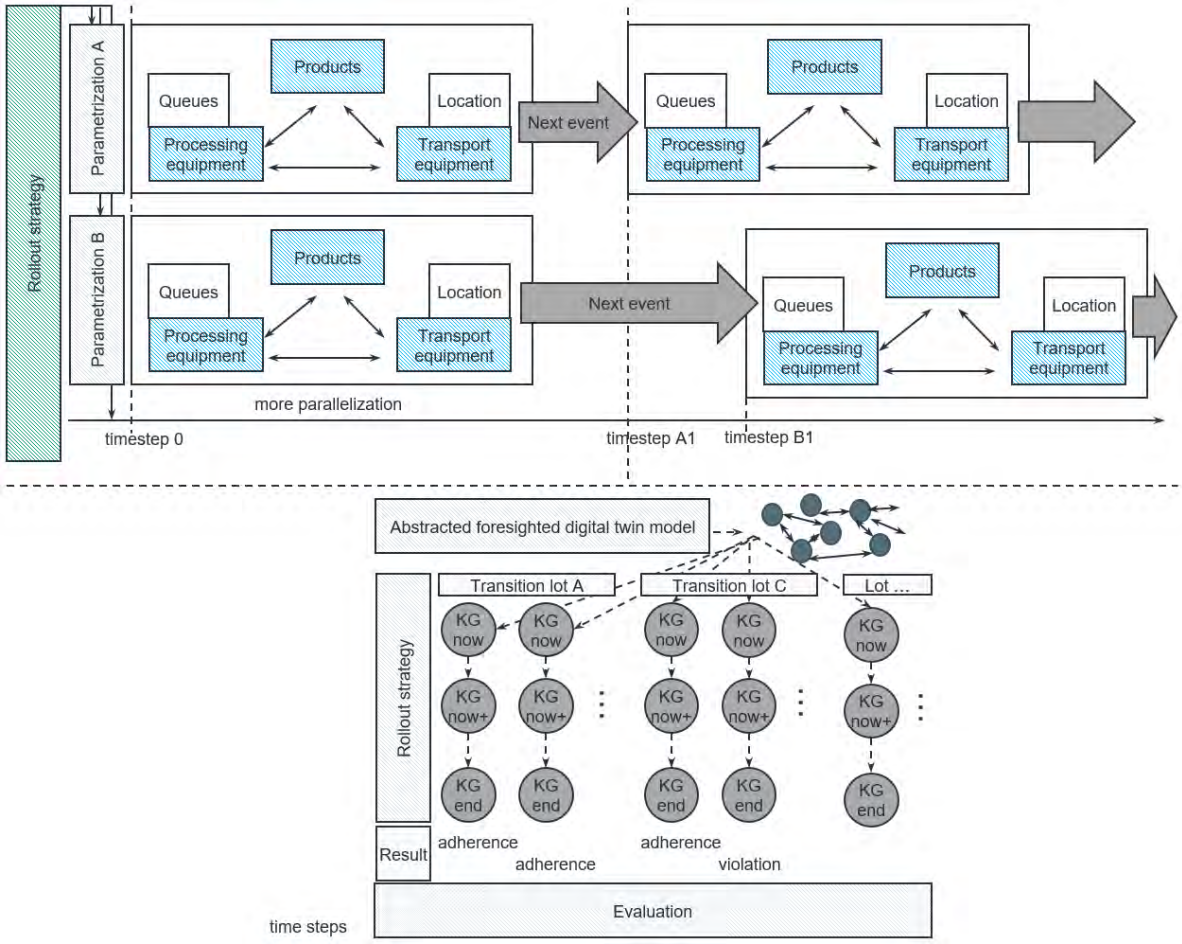

Figure 5: Rollout strategy and behavior.

For the evaluation of these rollouts a minimum regret policy of not releasing any time constrained lot that is at least violating the maximum time limit once or multiple times can be selected. Due to the interrelations within a semiconductor fab and the complex nature of their behavior (May et al. 2021) it is very likely that most time constrained lots will not satisfy this condition and an infeasible control logic is implemented. Thus, using a violation probability based approach (May et al. 2021) has advantages. The violation probability is obtained from the rollout sampling and only if the time constraint violation risk does not exceed a specified value the lot can be released as visualized in Figure 6. The transition time probability distribution is estimated based on the rollout samples observed. An acceptable risk limit of exceeding the time constraint can be ex post evaluated to conform to the fab operations strategy. Such a hyperparameter tuning can be achieved according to the actual trade-off between correctly and incorrectly withhold time constrained lots (May et al. 2021). This makes up the decisional rule in so far as time constrained lots can only be released if their time constraint violation risk does not exceed the selected threshold.

5 VALIDATION

The proposed approach is validated in a real-world semiconductor fab based on ex post fab data for several months. Given the transition time based evaluation the approach is restricted to simple time constraints and timelink areas as complex time constraints require a more in depth analysis.

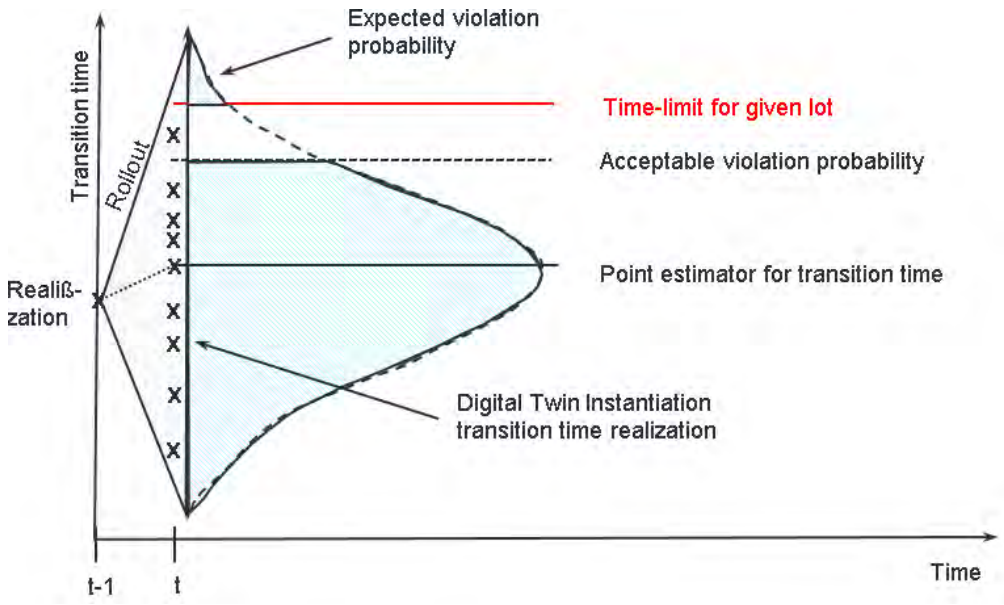

Figure 6: Evaluation of the time constraint violation probability and decisional rule.

Based on the ex post evaluation the model is compared to the real-world behavior in such a way that actual time constraint violations and adherences are re-evaluated and improvements over the state-of-the-art fab production control become visible following the approach of (May et al. 2024). Note that the dynamic nature of the decisional model leads to different decisions and results for an individual time constraint at different times so that withholding a lot at one decision does not mean it will be withhold for longer times. Table 1 shows the confusion matrix of the model's performance. More than two third of the actual violations, that would have occurred without any last minute interactions in the limited, regarded timeframe, could have been prevented with the proposed model showcasing the large improvement over the existing semiconductor fab control and manual interventions. However, a large number of lots is falsely predicted as a violation. Given the large, typically due to scrap, costs and environmental costs that come with any time constraint violation, the cost for short term falsely withholding a time constrained lot is almost negligible. Dominantly is that another, not time constrained lot is selected so that the throughput is not affected. In future work we will evaluate the effects on tardiness, what we clearly see in the validation is that a lot is not withhold for long as it is re-evaluated.

Table 1: Confusion matrix for the binary classification of time constraint violations with the proposed digital twin model

	Actual violation	Actual adherence
Predicted violation	21	681
Predicted adherence	10	2983

As a result the model can be positively validated as it indeed is capable of controlling the gate keeping decision of releasing time constrained lots in a semiconductor fab. It shows significant improvements over the state of the art in identifying violations, however, comes with a low precision. The low precision indicates a more conservative approach than the current control method, however, as proposed the evaluation of the rollout, here fine tuned with domain experts from the respective fab, can be adjusted. The decisional rule can be integrated in addition to the currently used method as additional measure by restricting the currents system choices with the proposed method. Thus, future work can improve both in the modeling and digital twin rollout as well as the actual decisional rule that is derived to improve precision.

6 CONCLUSION

The proposed approach to control the gate keeping of time constrained lots in semiconductor manfuacturing in a real-world setting and problem size is based on a digital twin that is instantiated multiple times to observe transition times and time constraint violations in the foresighted digital twin. Given the evaluation in this digital twin the actual release policy is constructed, based on a pre-selected maximum acceptable time constraint violation probability, where the probability is derived from the digital twin behavior observations. The model's real-world validation shows a reduction in time constraint violations of more than 67%, however comes at the cost of a large number of falsely predicted violations. The proposed methods validation is with ex post data so that real violations are re-evaluated ex ante to confirm the approaches efficacy. As a follow up the integration into the real fab is outstanding and to be reported in future papers. In Future work can improve the approach on the digital twin level, decision rule and possibility to include complex time constraints and evaluate their violation probability.

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