

FAB SIMULATION WITH RECIPE ARRANGEMENT OF TOOLS

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ABSTRACT

Presented in this paper is a FAB simulation framework considering the recipe arrangement problem of FAB tools. It is known that the WIP fluctuation is mainly caused by improper dispatching rules. Practical point of view, however, there is another cause of the WIP imbalance. We call the problem as a “recipe arrange problem of tools”. A FAB consists of multiple tool groups, and each tool group has multiple tools (machine devices). Currently, FAB tools belonging to the same tool group are assumed to perform the same set of recipes (operations). Practically, however, this is not true. Since FAB tools are extremely sensitive, tools even belonging to the same tool group are assigned different recipes with high yield. We developed a simulation model including the recipe arrangement problem by modifying MIMAC6, and conducted simulation with SEEPLAN® developed by the VMS solutions. The simulation result shows that it is necessary to have not only dispatching rules, but also arranging rules are required to minimize the WIP fluctuations in a FAB.

1 INTRODUCTION

Almost all everyday electrical and electronic devices includes semiconductor devices (integrated circuits) which are created by multiple-step sequence of photolithographic and chemical processing steps during which electrical circuits are gradually created on a wafer made of pure semiconducting material, Silicon. The entire manufacturing process, from start to packed chips ready for shipment, takes six to ten weeks and is performed in highly specialized facilities referred to as FABs.

A FAB is a highly automated manufacturing system, and requires a few billion dollars of investment. Strong competition, short product life cycle and increased complexity of products and processes are the characteristics of today’s FAB industry. Considering the characteristics, manufacturers need to continuously improve their products, as well as their production systems. Usually, a FAB consists of very expensive machines, and produces a large number of different product types concurrently, 24 hours a day. There are various constraints and re-entrant flows which enable such expensive machines to be shared by

many lots requiring the particular processing operation provided by the machine. To be successful in the globalized competition, full-capacity production for high utilization and just-in-time production for on-time delivery with minimum WIP (work-in-process) are essential in the FAB industry.

Much research on dispatching rules and scheduling optimization for FAB has been conducted, and several commercial packages are reported (Ko et al. 2010). Previous approaches on the FAB operation can be classified according to the KPIs (Key Performance Index); minimization of the cycle time, management of appropriate WIP levels (Work In Process), maximization of the utilization of critical tools, and on-time delivery considering due dates. Quek et al. (2007) proposed a dispatching rule to minimize efficiency loss. They tried to minimize the investment cost by optimizing the efficiency of critical tools. Chung and Jang (2009) considered the FAB scheduling problem as a static combinatorial problem, and developed LP (linear programming) methods for the maximization of the throughput. Other than the throughput issue, the balancing WIP is also an important performance indicator because the WIP imbalance can cause serious problems in terms of the cycle time and on time delivery. To solve the problem, there are various classical techniques like FIFO (First In First Out), CR (Critical Ratio), ODD (Operation Due Date), and EDD (Earliest Due Date). Lee and Lee (2003) suggested three different policies (push, push-pull, and pull type) to control WIP levels. Zhou and Rose (2010) proposed a WIP control table in order to balance the workloads of tools in a wafer FAB. Although there have been numerous research results on the dispatching rules and scheduling optimization for FAB, still FABs are suffering from the WIP imbalance problems (Zhou and Rose 2012). Since the WIP fluctuation has great impact on cycle time and on-time delivery, it is very important to achieve the smooth WIP flow and a low WIP level.

Our approach is not to develop a new dispatching rules or optimization techniques for the WIP balancing problem. Theoretically, the WIP fluctuation is mainly caused by improper dispatching rules. From a practical point of view, however, there is another cause of the WIP imbalance. We call the problem as an “arrange problem of tools”. A FAB consists of multiple tool groups, and each tool group has multiple tools (machine devices). Currently, FAB tools belonging to the same tool group are assumed to perform the same set of recipes (operations). Practically, however, this is not true. Since FAB tools are extremely sensitive, tools even belonging to the same tool group are assigned different recipes with high yield. Some researchers depicted this problem. Aron et al. (2008) proposed a yield sensitive dispatch to maintain high yield across all products while enhancing fab productivity and keeping costs down.

Figure 1 shows a tool group consisting of three tools, and the tool group performs four different recipes. Although the three tools are capable of performing all recipes, there are differences in terms of the yield rate for each recipe. To achieve high yield, recipes are usually assigned to different tools promising better yield. For example, Tool_1 is arranged for Recipe_1 and Recipe_3, while Tool_2 is just arranged for only one recipe, Recipe_2. If operators want to change the recipe arrangement, then it requires a specific setup time, from couple of minutes to couple of days. To improve the fidelity of FAB simulation, it is necessary to consider the arrangement problem.

To prevent the WIP fluctuation, it is necessary to analysis the WIP levels of tool groups, as well as those of recipes. The objective of this paper is to propose a FAB simulation model including the recipe arrangement problem of tools. The proposed simulation model shows the WIP level of each recipe in order to handle the arrangement problem of tools. For the execution of the model, we used a commercial software SEEPLAN® developed by the VMS solutions (Ko et al. 2010). The overall structure of the paper is as follows. Section 2 describes the FAB simulation model based on the MIMAC6 dataset from Measurement and Improvement of MANufacturing Capacities (MIMAC). Section 3 shows the simulation results and analysis on the WIP levels of recipes. Finally, concluding remarks are given in Section 4.

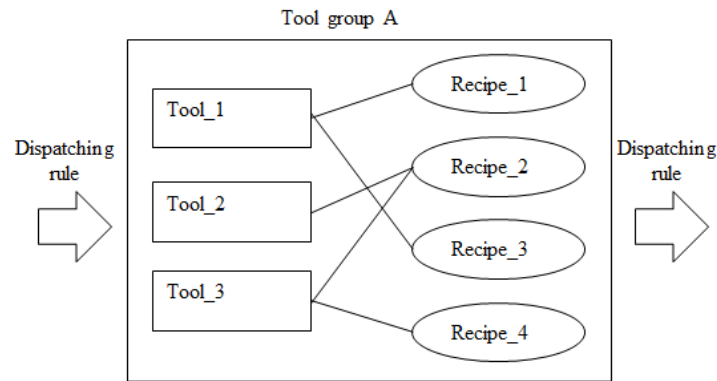


Figure 1: Recipe assignment of FAB tools

2 FAB SIMULATION MODEL INCLUDING ARRANGEMENT

We construct the simulation model by using the small wafer fab dataset MIMAC6 (Fowler and Robinson 1995). The FAB consists of 104 tool groups, and produces 9 products having different process steps. The total number of steps is 2541, and the average number of steps of products is 282. The product having longest steps has 355 steps, and the shortest one has 247 steps. The average processing time of steps is 3014 sec. The FAB consists of 104 tool groups, and total number of tools is 228. Each tool group may have multiple tools, from 1 to 10 in MIMAC6. A lot consists of 24 wafers, and 2777 lots are released per year under fab loading of 100%.

Based on the MIMAC6, we constructed two different models, FAB_A & FAB_B. While FAB_A is the original MIMAC6, FAB_B is modified to consider the recipe arrangement problem of FAB tools. Since FAB_A does not include the arrangement issue, FAB_A considers all tools, belonging to the same tool group, to be homogeneous. Our objective is to have some insights on the recipe arrangement problem by analyzing the simulation results of FBA_A and FAB_B.

To conduct the simulation of the two FABs, we employed the SEEPLAN® developed by the VMS solutions (Ko et al. 2010). Figure 2 shows how the SEEPLAN® engine generates loading schedule for each tool in the FAB. It requires three master data: bill of process (BOP) model, resource model, and dispatching rule. The current WIP is initialized at the beginning of simulation. Considering the current WIP, release plan is used as an input. The simulation results can be analyzed to see the key performance indices (KPI) including resource utilization, throughput, and WIP fluctuations.

BOP model is a network model which combines BOM (bill of material) and process routing. It consists of parts, processes, and transitions. We refer the interested readers to Ko et al. 2010 for details. BOP model contains step sequence, loadable resource list, and tact/flow time for each step, and average transfer time. A resource is characterized by handling unit, process type, and defect treatment policy. Resource group (tool group) indicates standard step to be processed, jig capacity, setup crew capacity, and list of unit resources (tools). Each resource has dispatching rule and tact/flow time. Dispatching rules are used to determine the priority for fulfilling orders. Typical examples of dispatching rules are first-in-first-out (FIFO), earliest-due-date (EDD), and shortest processing time (SPT). As shown in Figure 3, MIMAC6 data set is imported into SEEPLAN®.

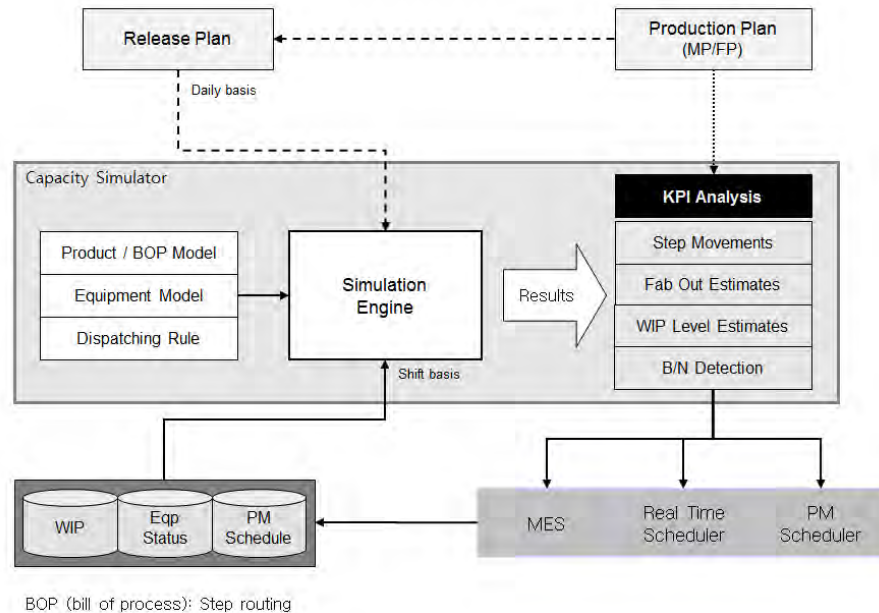


Figure 2: Forward Planning of SEEPLAN®

3 SIMULATION RESULTS

As, mentioned above, we developed two different models to analyze the effect of recipe arrangement problem. While FAB_A is the original MIMAC6, FAB_B is modified to consider the recipe arrangement problem of FAB tools. Each tool group has a set of steps (recipes), and tools of FAB_A are set to perform all steps of the tool group. On the other hand, tools of FAB_B are set to cover only 60 % of steps of the tool group. Figure 4 shows the WIP evolution curves of FAB_A & FAB_B. As expected, FAB_A shows much better WIP evolution curve, because FAB_B has much more tight constraints in terms of the recipe arrangement. Although FAB_A looks much better, the situation rarely happens in a real FAB consisting of extremely sensitive tools. For many practical reasons (machine failure, parameter adjustment, yield rate), tools are assigned different recipes with high yield.

Conventionally, the WIP evolution curves are analyzed only with respect to tool groups, because tools belonging to the same tool group are assumed to be homogeneous. Since we include the recipe arrangement issue in the simulation model, it is necessary to analyze the WIP evolution curves with respect to steps (recipes). In other words, the bottleneck should be identified in terms of steps not tool groups.

To show the effect of recipe arrangement problem, we chose four tool groups, 11129_ASM_F1_F2 (8 steps), 14021_AMC-EPI_1+2 (3 step), 15131_LZZZZ (28 steps), and 17421_HOTIN (1 step). The four tool groups include 12 steps, as shown in Table 1. Figure 5 shows the WIP evolution curves of FAB_B with respect to tool groups. From the WIP evolution curve, we can identify the bottleneck tool group, 15131_LZZZZ. If we do not consider the recipe arrangement problem, we may simply change the dispatching rules to minimize the WIP fluctuations. But, there can be clear limitations without changing the recipe allocation of FAB tools, when the WIP fluctuations are caused by bottleneck steps rather than bottleneck tool groups.

The simulation has been performed with FIFO dispatching logic. Figure 6 shows the WIP evolution curves of FAB_B with respect to steps, rather than tool groups. In this case, we can identify the three bottleneck steps, 14801_N9604 (14021_AMC-EPI_1+2), 39301_O4101 (11129_ASM_F1_F2), and 17531_N4101 (15131_LZZZZ). If bottleneck steps are identified in the simulation result, then the bottle-

neck steps should be notified to operators. But, the recipe reallocation should be planned very carefully by considering practical factors, such as the expected yield and the set up time ranging from couple of minutes to couple of days. The final decision of the recipe reallocation should be done by the operator. In this case, we assumed that the cost of recipe rearrangement is not significant, and widened the bottleneck recipes (14801_N9604, 39301_O4101, and 17531_N4101) for corresponding machines. Figure 7 shows the improved WIP evolution curves of FAB_B after recipe rearrangement. The dashed arrows of Figure 7 denotes the reduction of the peak points of WIP evolution curves.

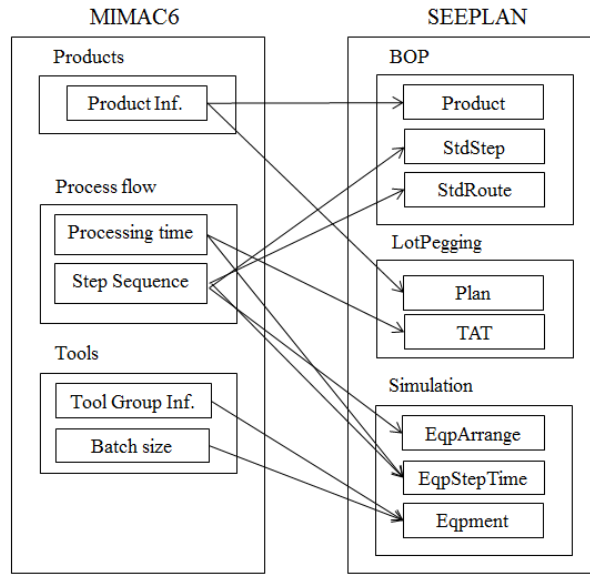


Figure 3: From MIMAC6 to SEEPLAN® model

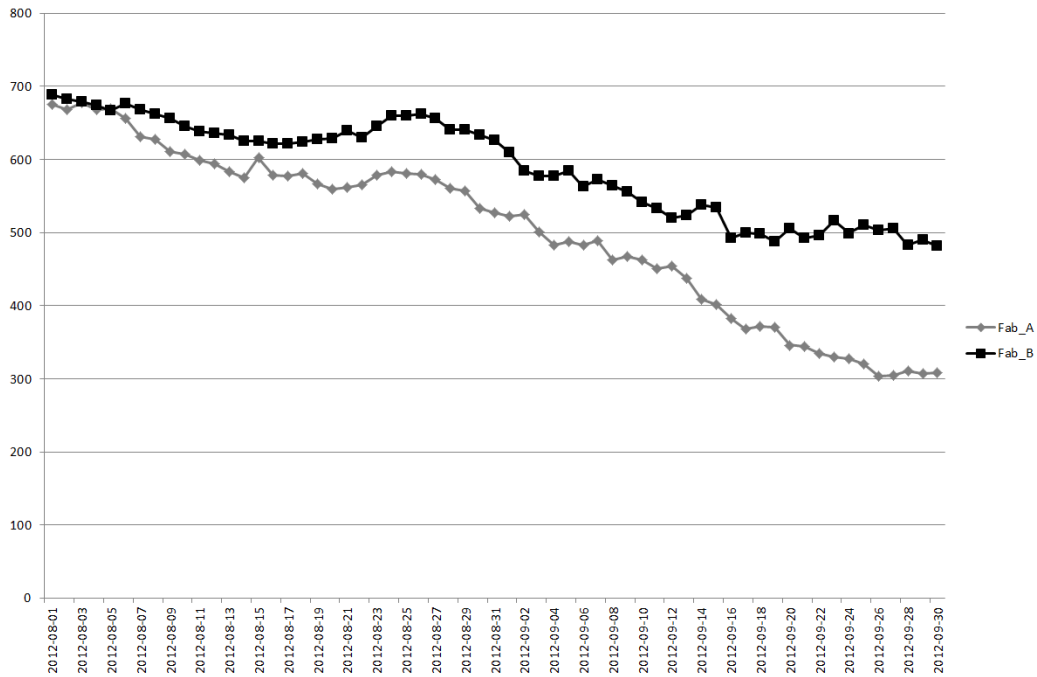


Figure 4: WIP evolution curves of FAB_A & FAB_B

Table 1: Tool groups & steps

Tool groups	Steps
11129_ASM_F1_F2 (8 steps)	39301_O4101 , 27241_O4104, 27241_O4101, 27241_O4103, 58201_O3204, 58201_O3512, 58201_XHLPL, 58511_O4102
14021_AMC-EPI_1+2 (3 step)	14801_N9604, 12501_N9605, 12501_N9606
15131_LZZZZ (28 steps)	11431_N4101, 12182_N4501, 13531_N4101, 13762_N4501, 14531_N4101, 17531_N4101, 18531_N4101, 19531_N4101, 20391_N4101, 22531_N4101, 24431_N4101, 25331_N4101, 26531_N4101, 28531_N4101, 32531_N4101, 32831_N4101, 33831_N4101, 41431_N4101, 41602_N4501, 43531_N4101, 45631_N4101, 47531_N4101, 48531_N4101, 49431_N4101, 50731_N4101, 51431_N4101, 53531_N4101, 59531_N4101,
17421_HOTIN (1 step)	75901_P5001

Figure 8 shows the proposed simulation framework including the recipe arrangement problem. The framework consists of four major steps; 1) simulation model execution, 2) analysis of WIP evolution curves with respect to steps, 3) identification of bottleneck steps, and 4) planning recipe rearrangement. In this paper, we simply identified the bottlenecks by considering only WIP levels. Step 3 & 4, however, involve various research issues, because it is necessary to consider many practical constraints and factors, such as due dates, moving rates, and recipe changing costs. It is a kind of deployment decision problem, and have been recognized by many researchers for many years (Bermon and Hood 1999).

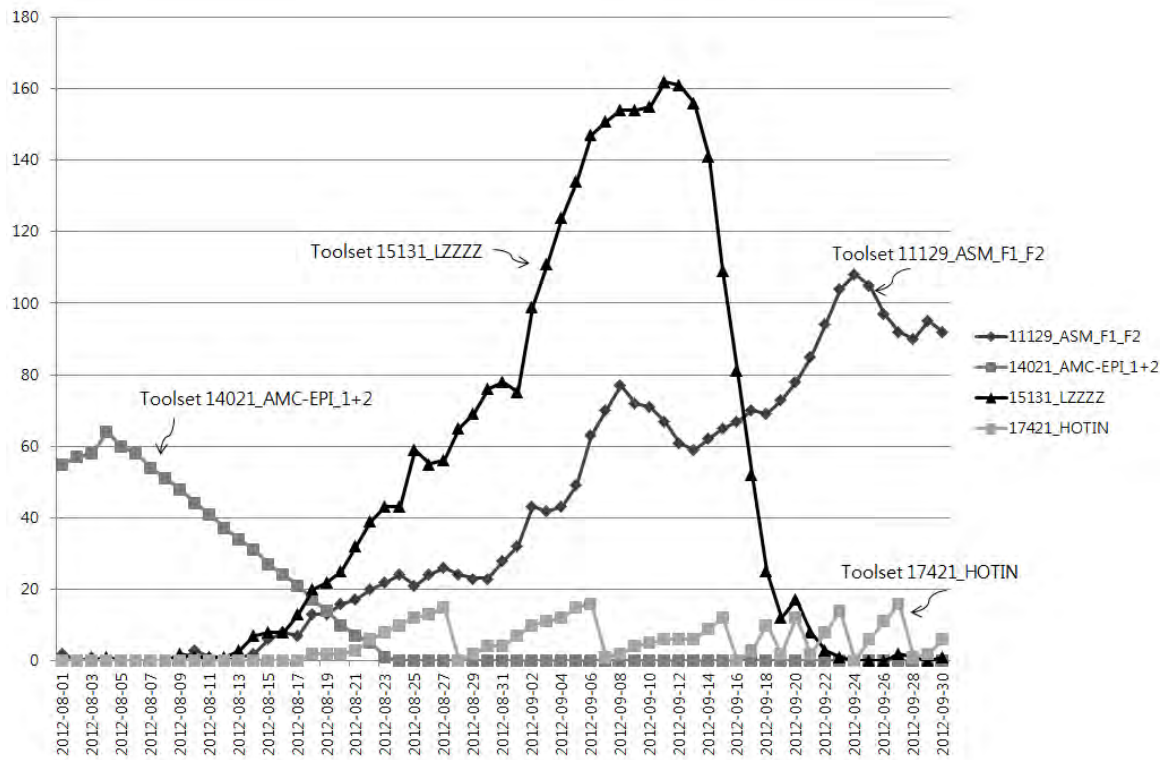


Figure 5: WIP evolution curve of FAB_B with respect to tool groups

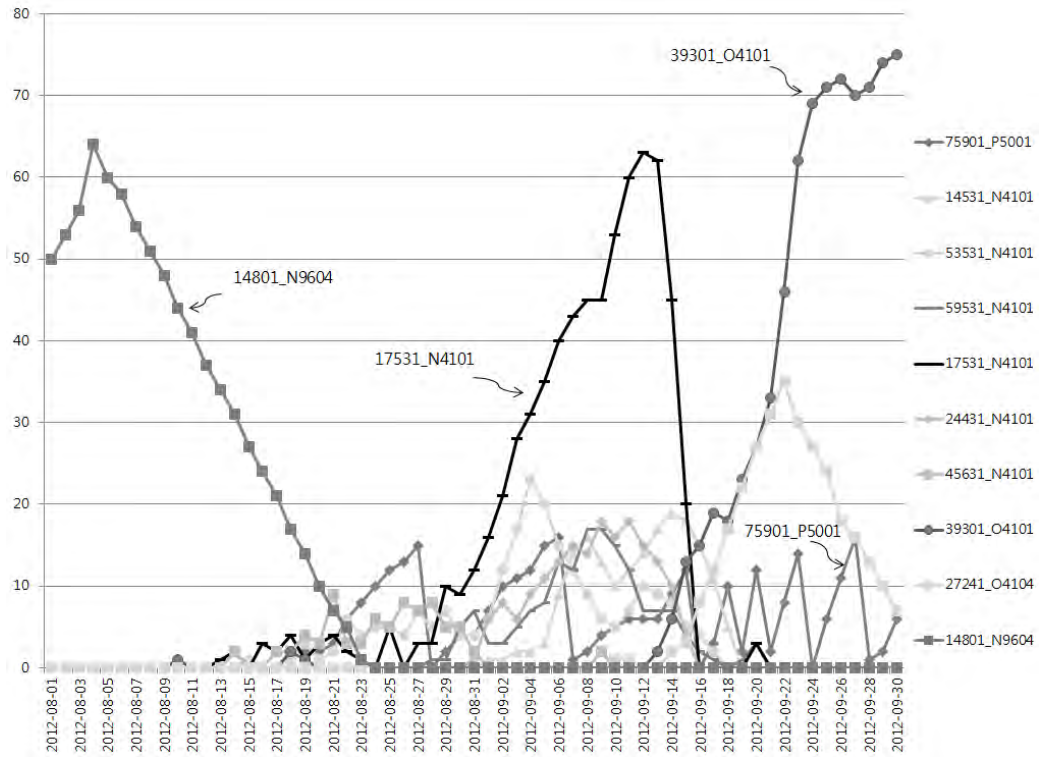


Figure 6: WIP evolution curve of FAB_B with respect to steps

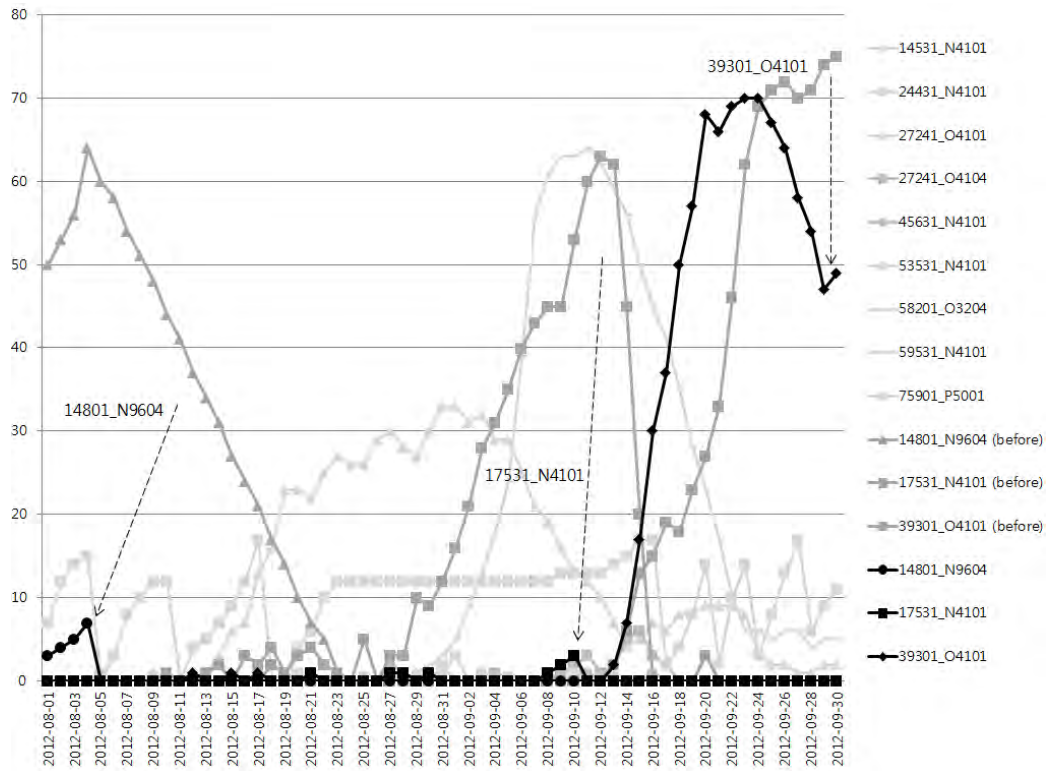


Figure 7: Improved WIP evolution curve of FAB_B after recipe rearrangement

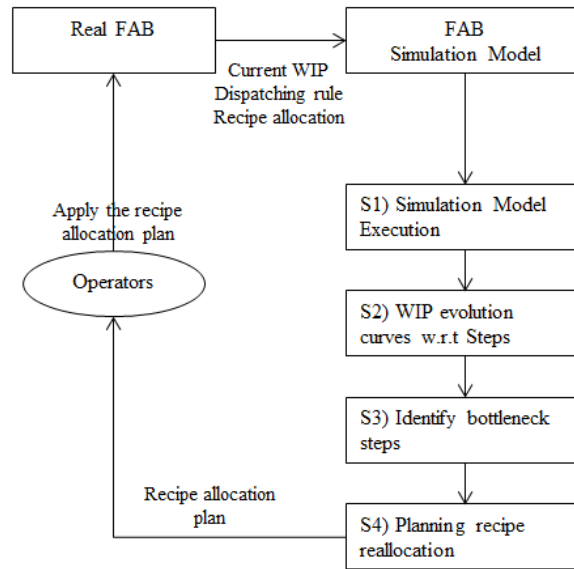


Figure 8: Simulation framework considering the recipe arrangement

4 SUMMARY

A FAB is a highly automated manufacturing system, and much research on dispatching rules and scheduling optimization for FAB has been conducted. There are various KPIs (Key Performance Index) for a FAB. Among various KPIs, WIP balancing is one of the most important performance indicators because the WIP imbalance can cause serious problems in terms of the cycle time and on time delivery. Although, it is known that the WIP fluctuation is mainly caused by improper dispatching rules, we identify another cause, the recipe arrangement problem. A FAB consists of multiple tool groups, and each tool group has multiple tools (machine devices). Currently, FAB tools belonging to the same tool group are assumed to perform the same set of recipes (operations). Practically, however, this is not true. Since FAB tools are extremely sensitive, tools even belonging to the same tool group are assigned different recipes with high yield.

We developed a simulation model including the recipe arrangement problem by modifying MIMAC6, and conducted simulation with SEEPLAN® developed by the VMS solutions. The simulation result shows that it is necessary to have not only dispatching rules, but also arranging rules are required to minimize the WIP fluctuations in a FAB. To include the recipe arrangement issue, we propose a simulation framework considering the recipe rearrangement consisting of four major steps. Among the four steps, the optimization of step 3 & 4 requires further research.

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REFERENCES

- Aaron, H.D., Krott L.C., Doxsey J. C. (2008). Optimizing yield and wafer Fab productivity through yield sensitive dispatch. *IEEE Transactions on Semiconductor Manufacturing* 21:318-321.
- Bermon S., and Hood S. (1999), Capacity optimization planning system (CAPS), *Interfaces* 29(5): 31-50.
- Choi, B.K., and N.K. You. 2006. Dispatching rules for dynamic scheduling of one-of-a-kind production. *International Journal of Computer Integrated manufacturing* 19:383-392.
- Chung, j., and J. Jang. 2009. A WIP balanced procedure for throughput maximization on semiconductor fabrication. *IEEE Transactions on Semiconductor Manufacturing* 22:381-390.
- Ko, K., B.C. Park, S.K. Yoo, E.S. Park, and B.H. Kim. 2010. Simulation based FAB scheduling: SEEPLAN®. In *Proceedings of the 2010 Winter Simulation Conference*, Edited by B. Johansson, S. Jain, J. Montoya-Torres, J. Hukan, and E.I Yucesan, 40-48. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers, Inc.
- Lee, Y.H. and Lee, B.J., Push-pull production planning of the re-entrant process, *International Journal of Advanced Manufacturing Technology*, 2003, 22: 922-931.
- Fowler, J., and J. Robinson. 1995. Measurement and Improvement of Manufacturing Capacities (MIMAC): Final report. Technical Report 95062861A-TR, SEMATECH, Austin, TX
- Quek, P.T., B.P. Gan, S. L. Tan, and C. L. Peng. 2007. Analysis of the front-end wet strip efficiency performance for productivity. In *Proceedings of International Symposium on Semiconductor Manufacturing, 2007, ISSM 2007*, 1-4
- Zhou, Z, and O. Rose. 2010. A pull/push concept for tool group workload balance in a wafer Fab. In *Proceedings of the 2010 Winter Simulation Conference*, Edited by B. Johansson, S. Jain, J. Montoya-Torres, J. Hukan, and E.I Yucesan, 2516-2521. Piscataway, New Jersey: Institute of Electrical and Electronics Engineers, Inc.
- Zhou, Z, and O. Rose. 2012. WIP control and calibration in a wafer FAB. In *Proceedings of the 2012 Winter Simulation Conference*, Edited by C. Laroque, J. Himmelspach, R. Pasupathy, O. Rose, and A. M. Uhrmacher,**.

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