

DYANA: HLA-BASED DISTRIBUTED REAL-TIME EMBEDDED SYSTEMS SIMULATION TOOL

Vitaly A. Antonenko*, Evgeny V. Chemeritskiy*, Alevtina B. Glonina*, Igor V. Konnov**, Vasily N. Pashkov*,
Vladislav V. Podymov*, Konstantin O. Savenkov*, Ruslan L. Smeliansky*, Dmitry Yu. Volkanov*,
Vladimir A. Zakharov*, Daniil A. Zorin*

*Lomonosov Moscow State University, Moscow, Russia

**Vienna University of Technology, Vienna, Austria

ABSTRACT

In this paper we present DYANA, an HLA-based hardware-in-the-loop simulation tool. This tool is used for distributed Real-Time Embedded Systems (RTES) simulation. RTES models are described by Unified Modeling Language (UML) statechart diagrams. The statechart diagram is transformed into HLA-based Simulation Model (HSM). After translation into HSM we use CERTI as the simulation runtime. The statechart diagram is also transformed into a Network of Timed Automata (NTA). After translation into NTA we use UPPAAL for RTES model verification.

1 DYANA OVERVIEW

Development of embedded devices and of the RTES itself is a distributed process performed by several teams located in different organizations. The tool which support this process is needed. In this paper we present DYANA, a tool for simulation and verification of RTES. This tool is a new revision of DYANA simulation environment (Bakhmurov A. 1999). The key features of DYANA are: UML statecharts as the modeling language for RTES; unified notation for simulation and verification; Worst Case Execution Time (WCET) analysis using the Metamoc tool; OTF trace format for execution traces of models run in CERTI.

Figure 1 shows the main components of DYANA:

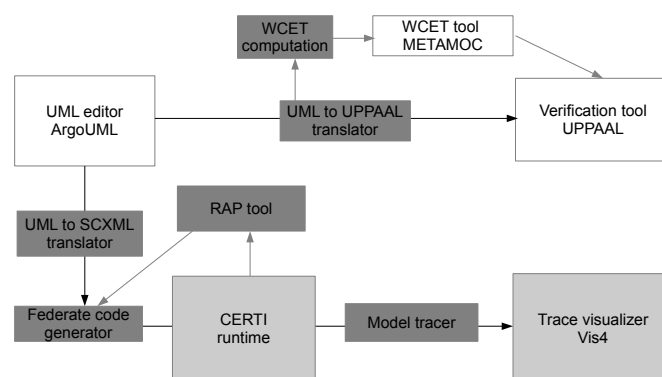


Figure 1: DYANA components

DYANA provides a specialized model development environment with a number of integrated services. Rectangles without background mark the tools that were integrated into DYANA as-is, rectangles with light background are modified tools and rectangles with dark background represent the tools developed specifically for DYANA.

ArgoUML is the UML editor used to create the models of real-time systems. Models are defined as UML statecharts. The models are saved to XMI format, so technically any UML editor that supports XMI can be used instead of ArgoUML.

UPPAAL is a verification tool. UML statecharts can be converted to UPPAAL format automatically in IDE. Correctness of this conversion showed in (Konnov I.V. 2012). During the conversion, WCET can be computed using Metamoc tool.

CERTI is the runtime for the real-time models. DYANA uses the modified multi-thread version of CERTI, different from the version on the trunk in the repository. UML models are automatically translated to HLA federates via the IDE. Model execution traces run in CERTI can be visualized in Vis4.

RAP tool is a tool for solving Reliability Allocation Problem for RTES (Bakhmurov A.G. 2011). Our RAP tool supports such methods as Evolutionary Algorithm, Simulation Annealing and Greedy Algorithm.

2 DYANA WORKFLOW

The way DYANA can be used for design of RTES can be illustrated by the following example. Suppose a flight controller system (Bakhmurov A.G. 2000) is under development, the whole code is not available yet, but the subsystem responsible for interprocessor communication and fault tolerance is ready. Then the general model can be simplified to include only the part relevant to the analysed subsystem. The resulting UML diagram is loaded in DYANA and converted to a net of UPPAAL timed automata. Then the safety and liveness properties of the system can be verified with UPPAAL checker.

If the checker finds a counterexample, the corresponding UPPAAL trace can be converted to a trace showing transitions in the original UML statechart. Using this trace, it is possible to modify the model to make it reproduce this trace every time. Then the model is converted to a set of federates in C++ and simulated in CERTI. The trace can be visualized in Vis4 to help the developers understand the problem discovered by the model checker.

3 FUTURE WORK

Directions for future research include :

- More thorough exploration of the proposed tool on data from real avionics systems.
- More strong cooperation between simulation and verification inside DYANA.
- Support HLA-based Hardware-In-The-Loop Simulation(HILS)
- Creation of tool for automated scaling of models for preparation for using of verification.
- Creation of tool for automated processing of simulation experiments results.

REFERENCES

- Bakhmurov A., e. a. 1999. "DYANA: An Environment for Embedded System Design and Analysis". In *Proc. of 5-th International Conference TACAS'99*, Volume 1579, 390–404. Amsterdam, The Netherlands.
- Bakhmurov A.G., e. a. 2000. "Towards a unified toolset for embedded systems development". In *Proceedings of the conference UKRPROG-2000 "Problems of Programming"*, 316–322. Kiev, Ukraine.
- Bakhmurov A.G., e. a. 2011. "Method For Choosing An Effective Set Of Fault Tolerance Mechanisms For Real-Time Embedded Systems, Based On Simulation Modeling". In *Problems of dependability and modelling*. Wroclaw, Poland.
- Konnov I.V., e. a. 2012. "On the designing of model checkers for real-time distributed systems". In *Program Semantics, Specification and Verification: Theory and Applications.*, 72–81. Nizhny Novgorod, Russia.